REMARKS

(1) Claims 1-9, 11-13, and 22-34 are pending in the present application. Applicant cancelled claim 10 herein. Applicant added new claim 34 herein, but no new matter has been added.

(2) The Office Action cited the following references:

A. U. S. Patent 6,313,024, by Cave, *et al.*, entitled *Method For Forming A Semiconductor Device* (referred to as "Cave, *et al.*" hereinafter);

B. U. S. Patent 6,261,944, by Mehta, *et al.*, entitled *Method For Forming A Semiconductor Device Having High Reliability Passivation Overlying A Multi-Level Interconnect* (referred to as "Mehta, *et al.*" hereinafter);

C. U. S. Patent 6,022,809, by Fan, entitled *Composite Shadow Ring For An Etch Chamber And Method Of Using* (referred to as "Fan" hereinafter); and

D. U.S. Patent 5,075,965 by Carey, *et al.*, entitled *Low Temperature Controlled Collapse Chip Attach Process* (referred to as "Carey, *et al.*" hereinafter).

(3) **Claim 10** has been rejected under 35 U.S.C. § 102(b) as assertedly being anticipated by Cave, *et al.* Applicant has cancelled claim 10 herein.

(4) Claims 12-13 and 22-26 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave, *et al.* Claims 1, 6-7, and 8-9 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave, *et al.* Claims 2-5, 11, and 29-33 were rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave, *et al* in view of Mehta, *et al.* Claim 27 was rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Cave, *et al*, as applied above, in view of Carey, *et al.* Applicant respectfully traverses these rejections for the following reasons. Claim 34 was newly added by this amendment. Regarding obviousness, MPEP 2143 (8th ed., rev. 2, May 2004) states:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the

art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

Claims 1-9

None of the cited references, either alone or in combination, disclose, teach, suggest, or motivate a "method of forming post passivation interconnects for an integrated circuit having a first plurality of contact pads in a first connection pattern," where the method comprises "forming a passivation layer over the integrated circuit and over the first plurality of contact pads, wherein the first plurality of contact pads could otherwise be used to provide electrical connection to an external component in packaging the integrated circuit by the formation of wire bonds or solder balls on the first plurality of contact pads, the passivation layer being formed from a non-oxide material," "forming a buffer layer over the passivation layer, the buffer layer comprising a silicon oxide layer," and "depositing a post passivation metal layer over the buffer layer after removing a top portion of the buffer layer," as claim 1 now requires. Accordingly, Applicant respectfully asserts that independent claim 1 is patentable over the cited references.

Because claims 2-9 depend from claim 1, Applicant respectfully submits that claims 2-9 are patentable over the cited references because of their dependency from independent claim 1 for the reasons discussed above.

If the rejection of claims 1-9 should be maintained, it is respectfully requested that the Patent Office point out with particularity how and where the cited references, either singularly or combined, disclose, teach, or suggest *all the claim limitations* of claims 1-9. In the absence of a *prima facie* showing of obviousness by the Patent Office, Applicant submits that claims 1-9 should now be allowed.

Claims 11-13 and 34

None of the cited references, either alone or in combination, disclose, teach, suggest, or motivate a "method of forming post passivation interconnects for an integrated circuit," where the method comprises "forming a passivation layer over a substantially complete integrated circuit and over a first plurality of contact pads, the first plurality of contact pads being in a first

connection pattern, wherein the passivation layer is formed from a non-oxide material," "forming an oxide buffer layer over and abutting the passivation layer, the oxide buffer layer having a thickness substantially smaller than a thickness of the passivation layer," and "forming a metal layer over the oxide buffer layer," as claim 34 requires.

The term "substantially complete integrated circuit" is defined and described in the patent specification. For example, while describing an illustrative embodiment (see e.g., FIGs. 1- 3b) of the present invention, paragraph [0022] provides: "Passivation layer 18 is the topmost layer of integrated circuit 10. This layer is formed after the circuitry of integrated circuit 10 is substantially complete. In other words, the circuits of the device are fully interconnected and operational when the passivation layer 18 is formed. The only remaining step is to provide access to power, ground and other signals so that the device can be coupled to other components." As another example, while describing an illustrative embodiment (see e.g., FIGs. 1-3b) of the present invention, paragraph [0034] provides: "The process begins with a substantially completed integrated circuit as shown in FIG. 1. In this context, a substantially completed integrated circuit is an integrated circuit that has been formed to the point that only connection to outside circuits is necessary to allow the device to operate as designed." A careful reading of the cited references, alone and in combination, will reveal that there is no mention, disclosure, or teaching of forming an oxide buffer layer over and abutting a passivation layer, which is over a substantially complete integrated circuit, and forming a metal layer over the oxide buffer layer. Accordingly, Applicant respectfully asserts that independent claim 34 is patentable over the cited references.

Because claims 11-13 depend from new claim 34, Applicant respectfully submits that claims 11-13 are patentable over the cited references because of their dependency from independent claim 34 for the reasons discussed above.

If the rejection of claims 11-13 and 34 should be maintained, it is respectfully requested that the Patent Office point out with particularity how and where the cited references, either singularly or combined, disclose, teach, or suggest *all the claim limitations* of claims 11-13 and 34. In the absence of a *prima facie* showing of obviousness by the Patent Office, Applicant submits that claims 11-13 and 34 should now be allowed.

Claims 22-28

None of the cited references, either alone or in combination, disclose, teach, suggest, or motivate a "method of forming a semiconductor device," where the method comprises "forming a nitride passivation layer overlying the uppermost metal layer except for selected contact openings to the first plurality of contact pads," "forming an oxide buffer layer overlying the nitride passivation layer," and "forming a post passivation metal layer overlying the oxide buffer layer, the post passivation metal layer patterned so as to electrically couple the first plurality of contact pads to a second plurality of contact pads formed in the post passivation metal layer," as claim 22 requires. Accordingly, Applicant respectfully asserts that independent claim 22 is patentable over the cited references.

Because claims 23-28 depend from claim 22, Applicant respectfully submits that claims 23-28 are patentable over the cited references because of their dependency from independent claim 22 for the reasons discussed above.

If the rejection of claims 22-28 should be maintained, it is respectfully requested that the Patent Office point out with particularity how and where the cited references, either singularly or combined, disclose, teach, or suggest *all the claim limitations* of claims 22-28. In the absence of a *prima facie* showing of obviousness by the Patent Office, Applicant submits that claims 22-28 should now be allowed.

Claims 29-33

None of the cited references, either alone or in combination, disclose, teach, suggest, or motivate a "method of forming a post passivation metal layer over an integrated circuit," where the method comprises "providing a substantially completed integrated circuit formed to the point that only connection to an external circuit would be needed to allow the device to operate," "forming an oxide buffer layer over and physically contacting the silicon nitride passivation layer," and "depositing a metal layer over and physically contacting the oxide buffer layer," as claim 29 requires.

The term "substantially complete integrated circuit" is defined and described in the patent specification. For example, while describing an illustrative embodiment (see e.g., FIGs. 1- 3b) of

the present invention, paragraph [0022] provides: "Passivation layer 18 is the topmost layer of integrated circuit 10. This layer is formed after the circuitry of integrated circuit 10 is substantially complete. In other words, the circuits of the device are fully interconnected and operational when the passivation layer 18 is formed. The only remaining step is to provide access to power, ground and other signals so that the device can be coupled to other components." As another example, while describing an illustrative embodiment (see e.g., FIGs. 1-3b) of the present invention, paragraph [0034] provides: "The process begins with a substantially completed integrated circuit as shown in FIG. 1. In this context, a substantially completed integrated circuit is an integrated circuit that has been formed to the point that only connection to outside circuits is necessary to allow the device to operate as designed." A careful reading of the cited references, alone and in combination, will reveal that there is no mention, disclosure, or teaching of forming an oxide buffer layer over and abutting a passivation layer, which is over a substantially complete integrated circuit, and forming a metal layer over the oxide buffer layer. Accordingly, Applicant respectfully asserts that independent claim 29 is patentable over the cited references.

Because claims 30-33 depend from claim 29, Applicant respectfully submits that claims 30-33 are patentable over the cited references because of their dependency from independent claim 29 for the reasons discussed above.

If the rejection of claims 29-33 should be maintained, it is respectfully requested that the Patent Office point out with particularity how and where the cited references, either singularly or combined, disclose, teach, or suggest *all the claim limitations* of claims 29-33. In the absence of a *prima facie* showing of obviousness by the Patent Office, Applicant submits that claims 29-33 should now be allowed.

(5) In view of the above, Applicant respectfully submits that the application is in condition for allowance and requests that the case be passed to issuance. If the Examiner should have any questions, Applicants request that the Examiner please contact Applicant's attorney at the address below. In the event that the enclosed fees are insufficient, please charge any additional fees required to keep this application pending, or credit any overpayment, to Deposit Account No. 50-1065.

Respectfully submitted,

1/12/05
Date

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